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EXAMINER	
CHO, JAMES HYONCHOL	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/727,106	KIEHL ET AL.	
	Examiner	Art Unit	
	James Cho	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,10,11,14-22 and 25-31* is/are rejected.

7)☒ Claim(s) *7-9,12,13,23 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the first and second bipolar transistors and the control circuit biasing the first and second bipolar transistors claimed in claim 26 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claims are objected to because of the following informalities:

In claim 1, "the at least one" on line 4 appears to be --at least one--;

In claim 6, "a first control" and "a control terminal" on line 2 appears to be --the first control-- and --the control terminal-- respectively, "a second control" and "a control terminal" on line 3 appears to be --the second control-- and --the control terminal-- respectively, and "the quiescent" on line 4 appears to be --a quiescent--;

In claim 7, "to a" on line 1 appears to be --to the--, "a control" on line 2 appears to be --the control--, "the quiescent" on line 3 appears to be --a quiescent--, "the switch" on line 4 appears to be --a switch--;

In claim 8, "the driver circuit" on line 4 appears to be --a driver circuit--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 26 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In substituting N-and P channel MOSFETs with npn, pnp bipolar transistors, the specification merely states that such a modification is "well understood in the art". The substitution of N and P channel MOSFETs, i.e. unipolar device with npn, pnp bipolar

transistors requires appropriate circuit modification since the current-voltage characteristics of MOSFET and bipolar transistor are different and simple substitution would make a circuit inoperable. The description relating to the control circuit is limited to MOSFET in the specification. The control circuit providing bias to a gate of a MOSFET would not work for providing bias to a base of a bipolar transistor since the MOSFETs and bipolar transistors has different current-voltage characteristics.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 14-20 and 27-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Roy et al. (US PAT No. 6,388,495).

Regarding claims 1 and 27, Fig. 6 of Roy et al. teaches an integrated circuit or a method comprising an active termination circuit (Fig. 6) having first and second transistors of opposite type coupled in series between a Vdd node of a first source potential and a Vss node of a second source potential (NMOS 120 and PMOS 155), the second source potential being lower than the first source potential (VDD and ground potential), the at least one termination node (105) being coupled to a common node (node where 120 and 155 commonly connected) between the first and second transistors and a control circuit operable to bias the first and second transistors (other components than 120, 155 in Fig. 6)

Regarding claim 2, Fig. 6 of Roy et al. teaches the integrated circuit of claim 1 where the control circuit is operable to bias the first and second transistors such that they provide a clamping function at the common node (col. 6, lines 19-22).

Regarding claims 3 and 29, Fig. 6 of Roy et al. teaches the integrated circuit/the method of claims 1 and 28 where the first transistor is a MOSFET of the N- channel type (NMOS 120) and the second transistor is a MOSFET of the P-channel type (PMOS 155); the drain of the first MOSFET is coupled to the Vdd node (VDD), and the drain of the second MOSFET is coupled to the Vss node (ground); and the sources of both MOSFETS are coupled together and to the common node (120 and 155 are commonly connected to a node).

Regarding claims 4 and 28, Fig. 6 of Roy et al. teaches the integrated circuit/the method of claims 1 and 27 where: the control circuit includes a first control terminal control circuit (130, 135, 140, 145, 150) operable to provide a first control terminal drive signal to a control terminal (gate of 120) of the first transistor, and a second control terminal control circuit (165, 170, 175, 180, 185) operable to provide a second control terminal drive signal to a control terminal of the second transistor (gate of 155), and the first and second control terminal drive signals are such that a quiescent voltage potential of the common node is between the Vdd and Vss potentials (the gate of 120 is

biased to Vtn and the gate of 155 is biased to VDD-Vtp which creates a quiescent current along the common node and a quiescent voltage; col. 6, lines 36-67).

Regarding claims 5 and 30, Fig. 6 of Roy et al .teaches the integrated circuit/the method of claims 4 and 27 where the quiescent voltage potential of the common mode is at about a midpoint between the Vdd and Vss potentials (when 120 and 150 are turned on by bias voltage, the intrinsic resistance 120 and 150 are about the same, which makes the voltage at the common node is about the half).

Regarding claim 6, Fig. 6 of Roy et al. teaches the integrated circuit of claim 4 where the first (130, 135, 140, 145, 150) and second (165, 170, 175, 180, 185) control terminal control circuits are operable to provide the first control terminal drive signal to the control terminal of the first transistor (gate of 120) and the second control terminal drive signal to the control terminal of the second transistor (gate of 155) to control a quiescent switch current through the first and second transistors (the gate of 120 is biased to Vtn and the gate of 155 is biased to VDD-Vtp which creates a quiescent current along the common node and a quiescent voltage; col. 6, lines 36-67).

Regarding clam 14, Fig. 6 of Roy et al. teaches the integrated circuit of claim 1 where the control circuit preferably includes a voltage source operable to produce a voltage of about a midpoint of the voltages of the voltage source Vdd and Vss (bias

generating circuit 130 and 150 produces Vtn, which is about a midpoint between VDD=1.9 volts to ground.

Regarding clam 15, Fig. 6 of Roy et al. teaches the integrated circuit of claim 1 where the control circuit preferably includes a voltage source operable to produce a voltage responsive to an externally supplied input voltage (internal bias generating circuit is based on VDD applied externally).

Regarding clam 16, Fig. 6 of Roy et al. teaches the integrated circuit of claim 1 and further comprising a resistor (the intrinsic resistance of the conductor between 105 and the common of 120 and 105).

Regarding claim 17, Fig. 6 of Roy et al. teaches an active termination circuit, comprising a first MOSFET (120) having a gate terminal, a drain terminal, and a source terminal, the source terminal coupled to a common node, and the drain terminal coupled to a Vdd node of a first source potential (VDD); a second MOSFET (155) having a gate terminal, a drain terminal, and a source terminal, the source terminal coupled to the common node, and the drain terminal coupled to a Vss node of a second source potential (ground), the second source potential being lower than the first source potential and a control circuit (other components than 120, 155 in Fig. 6) operable to bias the first and second MOSFETS.

Regarding claim 18, Fig. 6 of Roy et al. teaches the active termination circuit of claim 17 where the control circuit operates to bias the first and second MOSFETS such that they exhibit a controlled impedance at the common node (termination based on bias voltages; col. 6, lines 11-18).

Regarding claim 19, Fig. 6 of Roy et al. teaches the active termination circuit of claim 17, where the first MOSFET is an N-channel MOSFET (NMOS 120) and the second MOSFET is a P-channel MOSFET (PMOS 155).

Regarding claim 20, Fig. 6 of Roy et al. teaches the active termination circuit of claim 17, where the gate of the first MOSFET is coupled to a voltage source (VTN) between the Vdd and Vss potentials and the gate of the second MOSFET is coupled to another voltage source (VDD-VTP) of a lower potential.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 10-11, 15-18, 20, 22 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Bui et al. (US PAT No. 6,836,144).

Regarding claims 1 and 27, Fig. 1 of Bui et al. teaches an integrated circuit or a method comprising an active termination circuit (Fig. 1) having first and second transistors of opposite type coupled in series between a Vdd node of a first source potential and a Vss node of a second source potential (PMOS TPU, NMOS TDU), the second source potential being lower than the first source potential (VCCN and ground potential), the at least one termination node (155) being coupled to a common node (node where 141 and 142 commonly connected) between the first and second transistors and a control circuit operable to bias the first and second transistors (other components than 142, 142 in Fig. 1).

Regarding claim 10, Fig. 1 of Bui et al. teaches the integrated circuit of claim 1 and further comprising a third transistor (192) having a current path (channel between drain and source of 192) and a control terminal (gate of 192), the current path coupled between the first transistor and the voltage source Vdd (between VCCN and 141); and a fourth transistor (194), having a current path (channel between drain and source of 194) and a control terminal, the current path coupled between the second transistor and the voltage source Vss (between 142 and ground) where the operation of the first and second transistors can be selectively enabled or disabled by control signals (enable and /enable) coupled to the control terminals of the third and fourth transistors.

Regarding claim 11, Fig. 1 of Bui et al. teaches the integrated circuit of claim 10 where the third transistor is a P-channel MOSFET (192 PMOS) and the fourth transistor is a N-channel MOSFET (194 NMOS).

Regarding clam 15, Fig. 1 of Bui et al. teaches the integrated circuit of claim 1 where the control circuit preferably includes a voltage source operable to produce a voltage responsive to an externally supplied input voltage (internal bias generating circuit is based on VCCN applied externally).

Regarding clam 16, Fig. 1 of Bui et al. teaches the integrated circuit of claim 1 and further comprising a resistor (the intrinsic resistance of the conductor between 155 and the common of 141 and 142).

Regarding claim 17, Fig. 1 of Bui et al. teaches an active termination circuit, comprising a first MOSFET (141) having a gate terminal, a drain terminal, and a source terminal, the source terminal coupled to a common node, and the drain terminal coupled to a Vdd node of a first source potential (VCCN); a second MOSFET (142) having a gate terminal, a drain terminal, and a source terminal, the source terminal coupled to the common node, and the drain terminal coupled to a Vss node of a second source potential (ground), the second source potential being lower than the first source potential and a control circuit (other components than 141, 142 in Fig. 1) operable to bias the first and second MOSFETS.

Regarding claim 18, Fig. 1 of Bui et al. teaches the active termination circuit of claim 17 where the control circuit operates to bias the first and second MOSFETS such that they exhibit a controlled impedance at the common node (col. 2, lines 13-17).

Regarding claim 20, Fig. 1 of Bui et al. teaches the active termination circuit of claim 17, where the gate of the first MOSFET is coupled to a voltage source (bias voltage supplied by 121) between the Vdd and Vss potentials and the gate of the second MOSFET is coupled to another voltage source (bias voltage supplied by 122) of a lower potential.

Regarding claim 22, Fig. 1 of Bui et al. teaches the active termination circuit of claim 17 where the control circuit comprises: a first operational amplifier (115 coupled to the gate of 141 through 131) with an output coupled to the gate terminal of the first MOSFET; and a second operation amplifier (116 coupled to the gate of 142 through 132) with an output coupled to the gate terminal of the second MOSFET.

Regarding claim 25, Fig. 1 of Bui et al. teaches the active termination circuit of claim 17, and further comprising a first enable switch (192) coupled between the first MOSFET and Vdd (between 141 and VCCN) and a second enable switch (194) coupled between the second MOSFET and Vss (between 142 and ground).

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Omum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 17-18, 20-21 and 27-31 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-31 of copending Application No. 10/620,989. Although the conflicting claims are not identical, they are not patentably distinct from each other because they merely set forth the same claim limitations in slightly different claim language, and broad claims is clearly obvious over a narrow claims, e.g. first and second MOSFET vs. first and second N-channel MOSFET.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Allowable Subject Matter

Claims 7-9, 12-13, 21, 23-24 and 31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all

of the limitations of the base claim and any intervening claims as well as a timely filed terminal disclaimer as stated above with respect to claims 21 and 31.

The following is a statement of reasons for the indication of allowable subject matter: one of ordinary skill in the art would not have been motivated to modify the teaching of Roy et al. and/or Bui et al. to further includes, among other things, the specific of the first and second control terminal drive signals being controlled such that the quiescent current conducted through the switch is substantially less than the current through two resistors whose parallel resistance approximates the characteristic impedance of a coupled transmission line, the geometries, size and processing of the first and second transistors being scaled to achieve a controlled impedance and a quiescent voltage potential at the common node in response to an induced voltages, the first and second control terminal control circuits being capable of providing control terminal control signals that are greater than the source potential Vdd and less than the source potential Vss as set forth in claims 7-9 respectively, the specifics of a fifth transistor and a sixth transistor in series across a Vdd node of a first source potential and a Vss node of a second source potential and scaled to the first and second transistors', and a current source coupled to at least one of the fifth or sixth transistor that controls the quiescent current level in the first and second transistors as set forth in claim 12, the specifics of the potential difference between the voltage sources coupled to the gates of the first and second MOSFETS being controlled by a current source as set forth in claim 21, the specifics of the first and second operational amplifiers capable of producing gate drive signals greater than the power supply potential Vdd and less

than the power supply potential Vs respectively as set forth in claim 23, the specifics of scaling device geometries, device size, and processing of the first and second MOSFETS so that their coupled sources produce a controlled impedance and a quiescent voltage potential at the common node in response to an induced voltages produced by the driver circuit coupling communication signals to the termination node as set forth in claim 31.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Takizawa (US PAT No. 6,072,331) discloses an amplifier for active termination.

Drost et al. (US PAT No. 5,955,911) discloses on-chip differential resistance technique.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James H. Cho
Primary Examiner
Art Unit 2819

June 23, 2005